

PCI Express® Gen4 x8 OCuLink Interposer User Manual and Quick Start Guide

Before Starting

Use this document for quick installation and setup. If you experience problems or need more information, see the product manuals available at the Teledyne LeCroy web site <https://teledynelecroy.com/sw/pciexpress>.

1 Introduction

Teledyne LeCroy's PCI Express Gen4 x8 OCuLink Cable Interposer for the Summit™ PCI Express Protocol Analyzer product line provides individual dedicated probes, making it easy to capture and analyze data traffic between a host and device that are connected using a PCIe® OCuLink type cable based on the PCI Express OCuLink Cable specification. The PCI Express Gen4 x8 OCuLink Interposer taps into the OCuLink point to point connection to allow an analyzer to capture and decode data traffic between two systems. It supports data rates of 2.5 GT/s, 5.0 GT/s, 8.0 GT/s and 16.0 GT/s. The interposer assures reliable data transmission while providing 100% capture of all data traffic flowing through the PCIe interface. Connecting the interposer to a Teledyne LeCroy analyzer allows analyzer to decode and display data in both directions and across all lanes.

One PCIe OCuLink Cable can support PCIe link widths from x1 to x4. Larger links can be achieved by adding additional cables, e.g. a x8 link uses two PCIe OCuLink cables. The PCI Express OCuLink Specification allows in addition to in-band PCIe signaling the passage of sideband signals such as PERST#, WAKE# and SMBus by passing them electrically through the link. The sideband signaling (PERST#, WAKE#, SMBus and other functionality) can be monitored by the protocol analyzer through the interposer, where protocol issues and performance metrics can be analyzed and debugged. RefClk signals external to the cable are also available on the PCIe OCuLink Cable Interposer for use with the protocol analyzer.

The PCI Express Gen3 x8 OCuLink Interposer works with the PCIe OCuLink cable (or set of cables) up to 0.6 meter in length as defined in the PCI Express OCuLink Cable specification.



PCI Express Gen4 x8 OCuLink Interposer

2 Components

The interposer package includes the following components:

- PCI Express Gen4 x8 OCuLink Interposer
- PCIe OCuLink Internal Cables (Two PE017UCA-X cables 60cm each)
- DC Power Adapter (12 volts @ 5A)
- User Manual and Quick Start Guide (this document)

Inspect the received shipping container for any damage. Unpack the container and account for each of the system components listed on the accompanying packing list. Visually inspect each component for absence of damage.

In the event of damage, notify the shipper and Teledyne LeCroy. Retain all shipping materials for shipper's inspection.

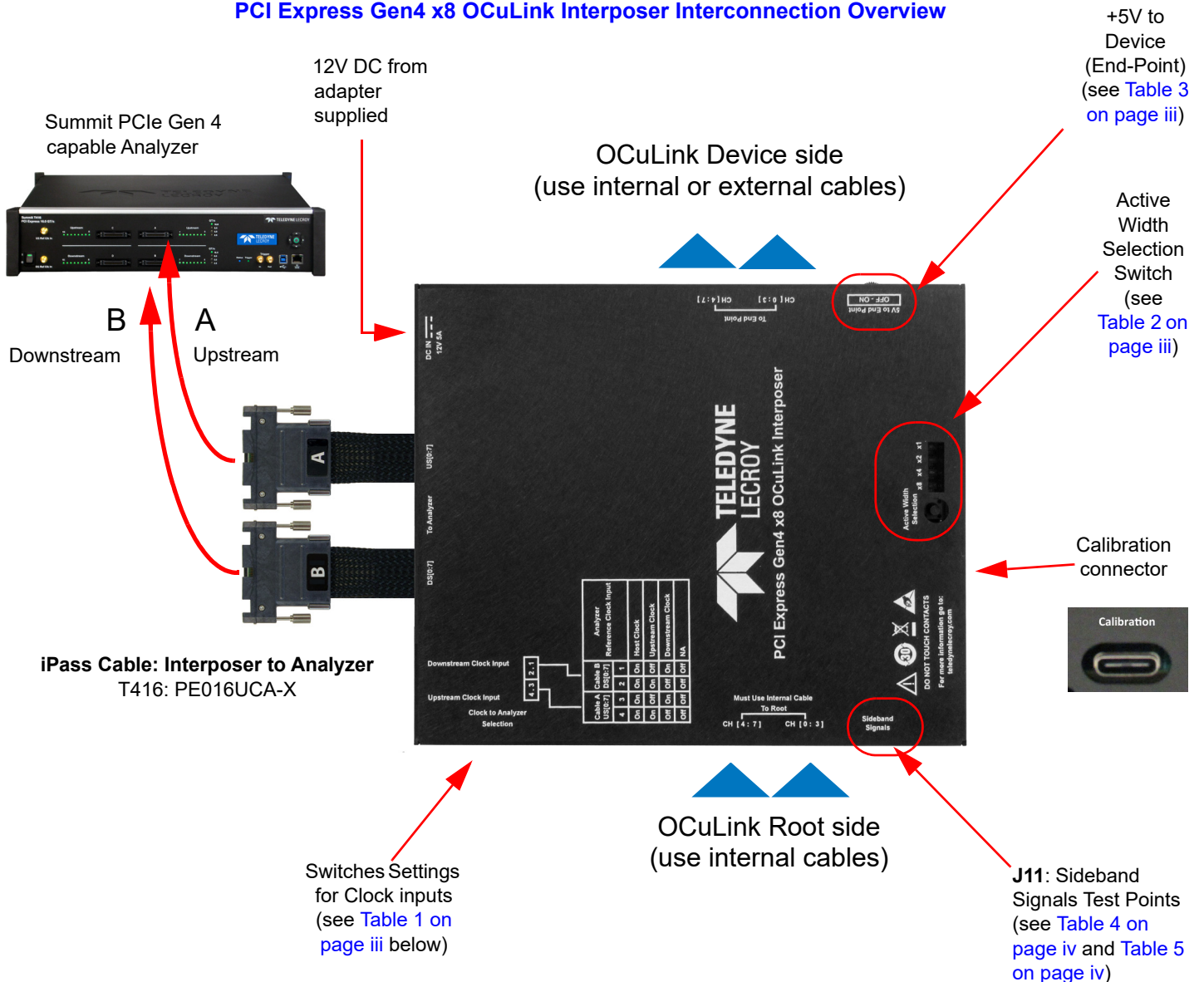
3 Connections

Perform to the following steps to connect the Interposer (see the image below):

1. Connect the supplied Teledyne LeCroy PCIe OCuLink Internal cable (PE017UCA-X) between the CH[0:3] port on the Root side of the interposer and Port-0 of the OCuLink root. If x8 configuration is required, connect both Teledyne LeCroy PCIe OCuLink internal cables between the Root side ports of the interposer and Port-0 and Port-1 of the OCuLink root.
2. If working in x4 configuration with an internal device, connect the second Teledyne LeCroy PCIe OCuLink Internal cable (PE017UCA-X) between the CH[0:3] port on the Device side of the interposer and Port-0 of the OCuLink device. If x8 configuration is required use two off-the-shelf cables to connect the End Point side ports from the interposer to Port-0 and Port-1 of the OCuLink device. If working with external devices you will need an off the shelf 0.6m external cable.
3. Connect the Summit PCIe Gen 4 capable analyzer to the interposer as indicated in the diagram below.
4. Install the PCIe Protocol Analysis Software on the host machine. This application is needed to control the protocol analyzer.
5. Connect the analyzer to a host machine (where the PCIe Protocol Analysis Software application will be running) using the USB or Ethernet port on the back panel of the Summit analyzer (or other compatible Teledyne LeCroy analyzer).
6. Connect 12V DC using the AC adapter supplied with the interposer. Make sure that the AC adapter is turned on.
7. Power on the analyzer.
8. Power on the host/root complex system.
9. Use the Teledyne LeCroy software application to monitor, record and view PCI Express traffic in the PCIe expansion card DUT system. Use Internal Clock in the recording options tab of the application. In order to improve lock time for analyzer provide reference clocks for upstream and downstream and use External Clock option.

Note: Steps 6, 7, and 8 are needed in this order for power on traces.

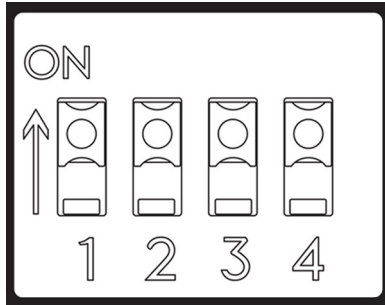
PCI Express Gen4 x8 OCuLink Interposer Interconnection Overview



4 Switch Settings: Clocks, Link Width, Power to Device

SW1 can be used to configure SRIS support by selecting the appropriate clock supplied to the analyzer system while recording traffic.

Table 1: Switch Settings for Clock Inputs and Cable Configurations: SW1



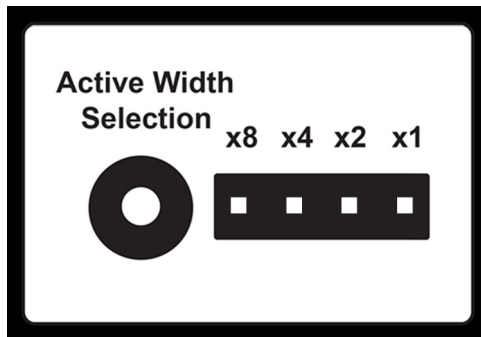
Cable A US[0:7]		Cable B DS[0:7]		Analyzer Reference Clock Input
SW1-4	SW1-3	SW1-2	SW1-1	
ON	ON	ON	ON	Host Clock
ON	OFF	ON	OFF	Upstream Clock
OFF	ON	OFF	ON	Downstream Clock
OFF	OFF	OFF	OFF	NA

Note 1: Factory settings for all switches are ON.

Note 2: Host Clock is sourced from the Root System OCuLink connector VSP pins A12/A13.

The Teledyne LeCroy PCIe Gen4 OCuLink is an active interposer and the probing circuitry has terminations at the input for each lane which acts as RX detection resistor. This feature on the circuitry also allows it to set the link width by selectively turning ON or OFF this termination resistor. Follow the table below and use the Active Width selection switch to set the appropriate link width.

Table 2: Switch Settings for Active Link Width Selection: SW3



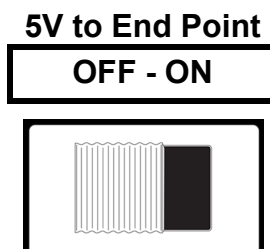
SW3	Active Link Width Selection Switch
x8	Link Width Set to 8
x4	Link Width Set to 4
x2	Link Width Set to 2
x1	Link Width Set to 1

Note: Factory settings for the switch is x8.

The Active Width Selection switch allows user to select the maximum link width to be used for traffic capture. Keep toggling the switch to cycle through all possible link widths: x1, x2, x4 and x8. An LED will indicate the current selection.

The device side connector on the PCIe Gen4 OCuLink Interposer supplies 5V on pins A21 and B1. In order to support both OCuLink internal and external crossover cables the interposer does not pass the 5V from HOST port to DEVICE port. The switch SW4 can be used to turn this power ON / OFF based on user's set up requirement.

Table 3: Switch Settings for +5V to Device (End-Point): SW4



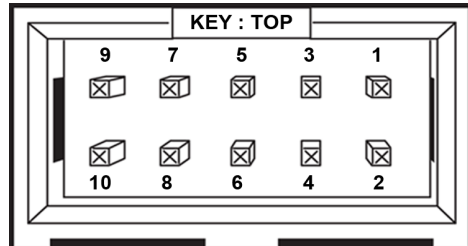
SW4	+5V Selector Switch to Device (End-Point)
OFF	No +5V to Device (End-Point)
ON	+5V to Device (End-Point)

Note: Factory setting for the switch is OFF.

5 Test Points

Test points are provided on sideband signals on the Interposer as a probing point. The Interposer passes all the sidebands through and does not change the behavior based on the state of the of the sideband signal. All the sideband signal's functionality are controlled by HOST and DEVICE and the Interposer is transparent to the sidebands.

Table 4: J11 Sideband Signal Test Points



PIN	DESCRIPTION	PIN	DESCRIPTION
1	CH[0:3] Port BP TYPE	6	CH[4:7] Port PERST#
2	CH[4:7] Port BP TYPE	7	CH[0:3] Port CPRSNT#
3	CH[0:3] Port CWAKE#	8	CH[4:7] Port CPRSNT#
4	CH[4:7] Port CWAKE#	9	GND
5	CH[0:3] Port PERST#	10	GND

Table 5: J11 Sideband Signal Descriptions

SIGNAL NAME	DESCRIPTION
BP TYPE	Input required to enable a full crossover internal cable solution.
WAKE#	Power management signal for Downstream device wakeup events.
PERST#	PCI Express Reset indicates when the applied main power is within the specified tolerance and is stable.
CPRESNT#	Cable present signal

6 Calibration/Debug Port

The Interposer has a standard USB Type C connector as a Debug/Calibration Port. The Calibration port allows the user to calibrate the proprietary circuitry on the interposer to get recovery free traffic between Host and Device and error free traffic recording on the analyzer. Connect a USB Type C to Type A cable to a host computer which runs the PCIe Protocol Analysis Software. Circuitry in the interposer has CTLE and DC gain settings on each lane towards DUT and to Analyzer path. The values for both CTLE and DC Gain range from 0.2 dB to 6.2 dB and can be changed in 0.2 dB steps. Increase or decrease both parameters independently or in tandem to achieve the recovery free and error free traffic recording. Factory default settings for CTLE and DC Gain are set based on the internal calibration set up and may not work with your particular set up. Follow the PCIe Protocol Analysis Software manual for more information on calibrating interposers.

7 Environmental Conditions

- Temperature: Operating 32° F to 122° F (0° C to 50° C)
- Temperature: Non-Operating 14° F to 176° F (-10° C to 80° C)
- Humidity: Operating 10% to 90% RH (non-condensing)

Teledyne LeCroy Customer Support

Online Download

Periodically check the Teledyne LeCroy Protocol Solutions Group web site for software updates and other support related to this product. Software updates are available to users with a current Maintenance Agreement.

Web: teledynelecroy.com/sw/pciexpress
E-mail: psgsupport@teledyne.com
Support: teledynelecroy.com/support/contact



Trademarks and Servicemarks

Teledyne LeCroy, PCIe Protocol Suite, PCIe Protocol Analysis, Summit T416 are trademarks of Teledyne LeCroy. All other trademarks are property of their respective companies.

Changes

Product specifications are subject to change without notice. Teledyne LeCroy reserves the right to revise the information in this document without notice or penalty.