PARADE TECHNOLOGIES INC.

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PS8570

16GT/s 4-Channel PCI Express Linear Redriver with Cross Switch

Version 0.71

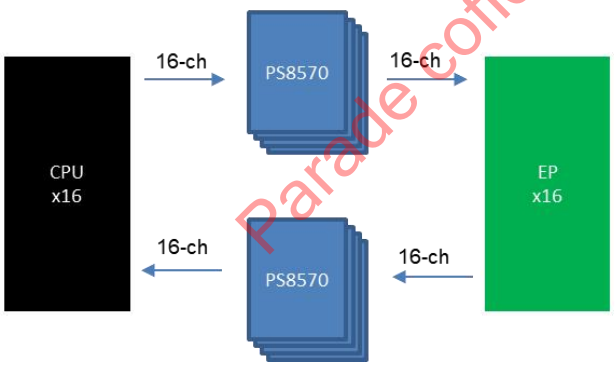
Apr 21, 2023

KEY FEATURES

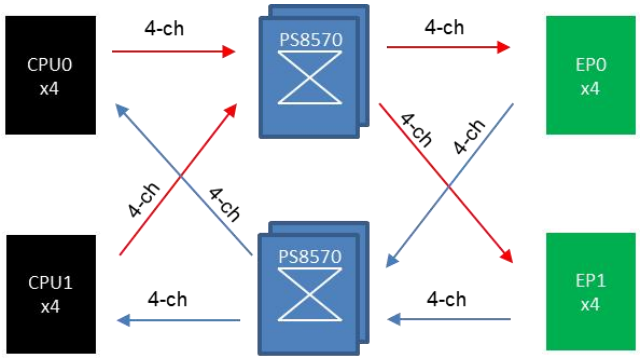
- Supports PCIe operation at 2.5GT/s, 5.0GT/s, 8.0GT/s and 16GT/s
- Supports PCIe link training and power management
- 2x2 crossbar switch
- Programmable equalizers
- Supports stack up for x8 or x16 link
- Low latency of 60ps
- Low additive jitter
- Supports L1PM feature
- Integrated automatic squelch function
- Low power consumption of 48mW/channel
- Supports SMBus/I2C configuration and external EEPROM configuration (optional)
- Single 1.8V power supply
- 2.8mm x 6mm 38-pin QFN halogen-free RoHS Package
- 0°C to 70°C operating temperature range for PS8570QFN38GTR-A1
- -40°C to 85°C operating temperature range for PS8570QFN38ITR-A1
- ESD: HBM 5KV

APPLICATIONS

- Desktop and laptop computers
- Servers
- Workstations



Normal Application



Crossbar Application

DESCRIPTION

PS8570 is a unidirectional 4-channel PCIe linear redriver that integrates programmable equalizers to re-condition PCIe signals. It can support PCIe Gen 4 speed up to 16GT/s data rate. It supports 2x2 cross-bar switching for various connections. PS8570 consumes low power in operation; no heat sink or fan requirement. PS8570 supports PCIe power management, particularly the L1PM power saving feature.

Equalization and DC gain

PS8570 provides programmable equalization at the receiving side to compensate for the signal loss caused by PCB traces and/or FPC cables and implements DC gain to keep redriver work in good condition.

PCIe link training

PS8570 has excellent linearity that ensures the output waveform still preserve its original characteristic. This feature makes PS8570 transparent at PCIe link training phase.

Automatic squelch

The input and output signals shall be AC coupled to PS8570. PS8570 integrates squelch circuits which will drive the output to common mode voltage when input signals fall below the threshold level at the input for each channel. This feature helps prevent un-needed signal repeating on PS8570.

L1PM feature

When the pin of CLKREQB is de-asserted, PS8570 will be shut down without any latency, and the power is very low under this condition. Once CLKREQB is asserted, PS8570 will return to normal operation mode quickly.

Cross-bar feature

PS8570 supports 2x2 cross-bar feature – neighboring two channels can be cross switched and output. With this feature, multiple connection topologies can be easily realized by using PS8570 to enable the applications of two RCs sharing with one EP, or two EPs sharing with one RC port, or two RCs sharing with two EPs.

Automatic power saving

PS8570 implements the automatic power saving feature which is particularly useful for power sensitive application. The power saving mode is channel based. When any channel is idle more than the predefined time, the channel will enter power saving mode automatically. When effective signal is detected, the channel will exit the power saving mode immediately and be able to function normally as a repeater.

FUNCTIONAL BLOCK DIAGRAM

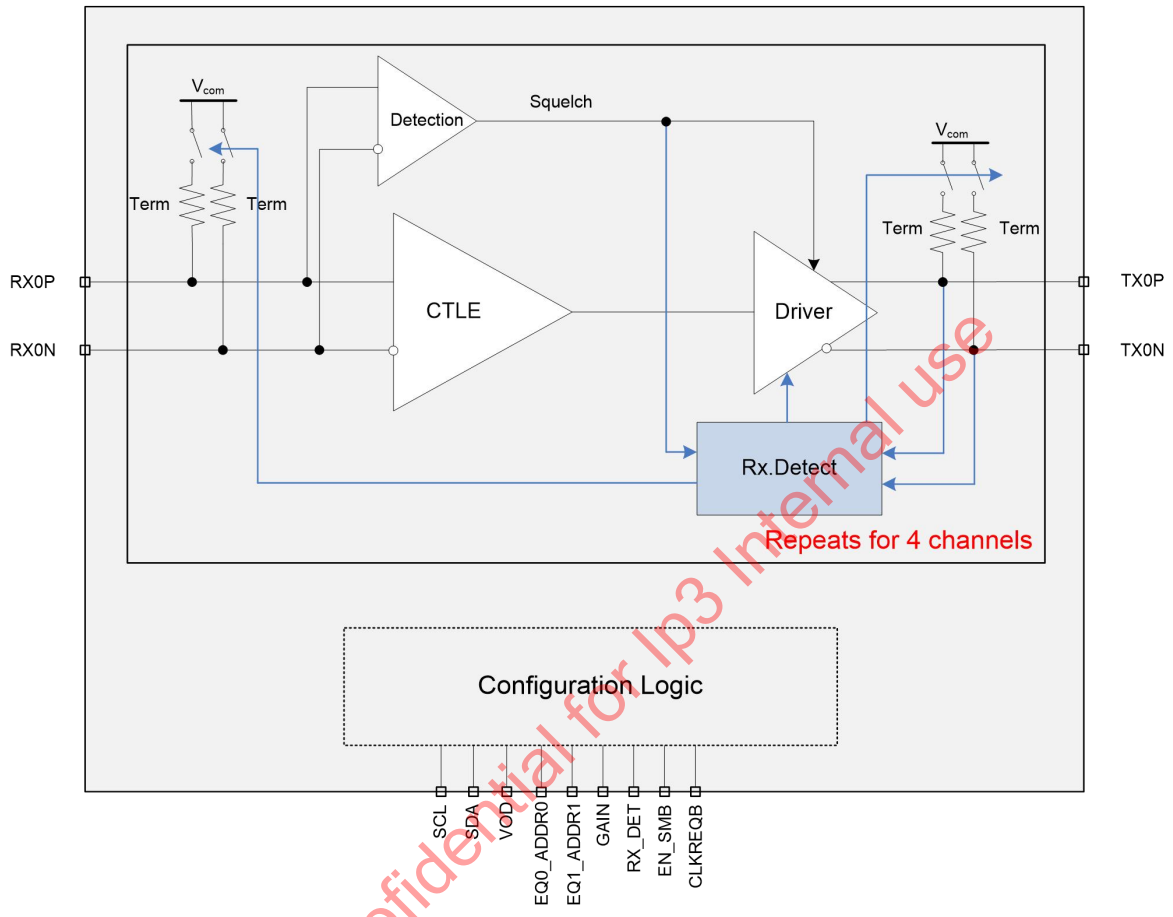


Figure 1. PS8570 Functional Block Diagram

CROSSBAR OPERATION DIAGRAM

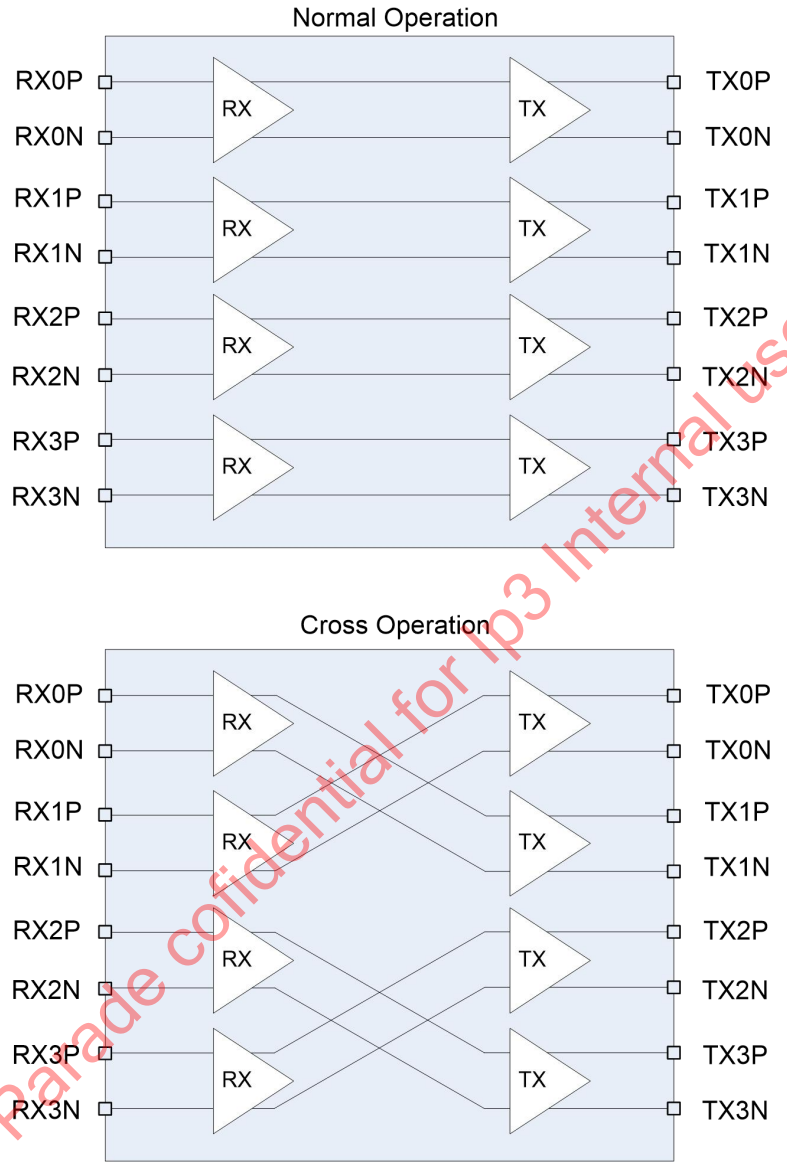


Figure 2. PS8570 crossbar feature diagram

PIN ASSIGNMENT & DESCRIPTION

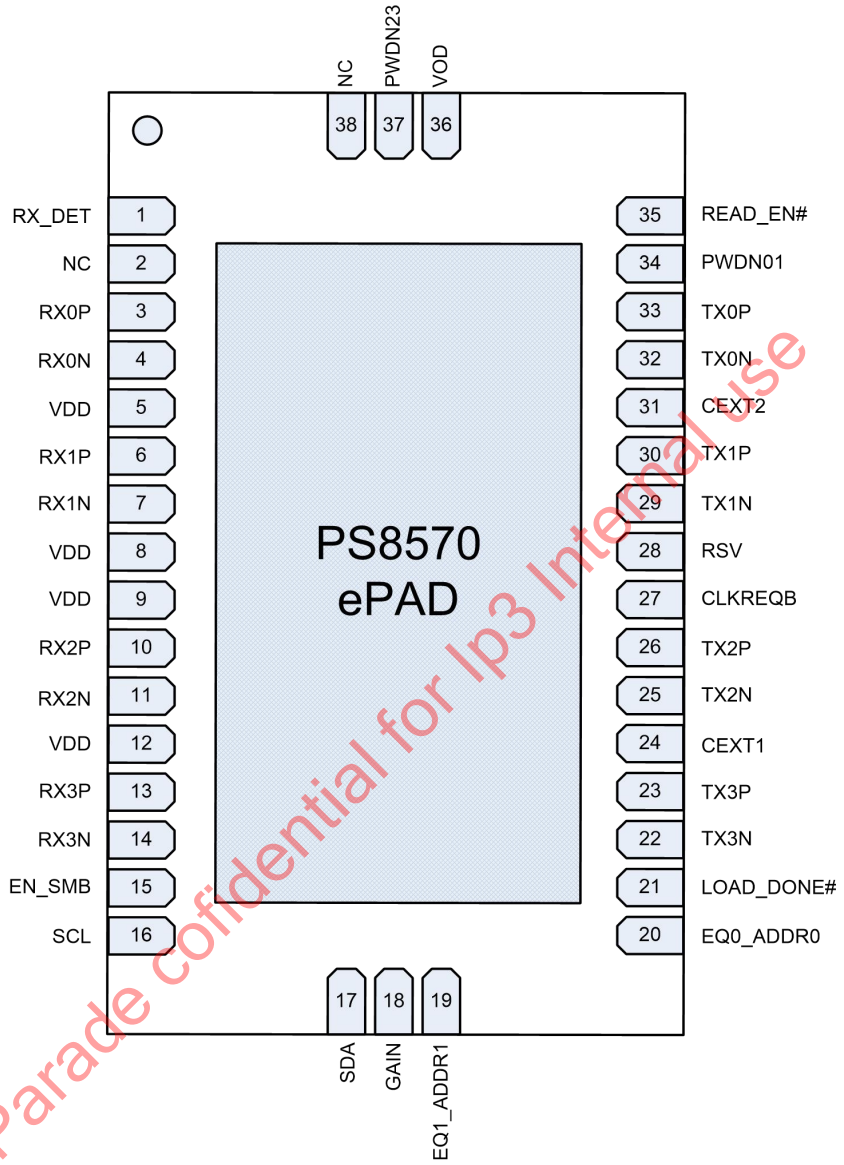


Figure 3. PS8570 Pin Assignment (Top View)

Table 1. PS8570 Pin Descriptions

Pin#	Name	I/O	Description
High speed differential I/Os			
3	RX0P	I	Receiver differential pair of channel 0
4	RX0N	I	
6	RX1P	I	Receiver differential pair of channel 1
7	RX1N	I	
10	RX2P	I	Receiver differential pair of channel 2
11	RX2N	I	
13	RX3P	I	Receiver differential pair of channel 3
14	RX3N	I	
33	TX0P	O	Transmitter differential pair of channel 0
32	TX0N	O	
30	TX1P	O	Transmitter differential pair of channel 1
29	TX1N	O	
26	TX2P	O	Transmitter differential pair of channel 2
25	TX2N	O	
23	TX3P	O	Transmitter differential pair of channel 3
22	TX3N	O	

Configuration pins

<table>
<tr><td>19</td><td>EQ1_ADDR1</td><td>I</td><td rowspan="2">EN_SMB = L0
Two pins work as EQ1 and EQ0 respectively. See Table 2 for EQ level options.

EN_SMB = L1/L2/L3/L4
Two pins work as ADDR1 and ADDR0 respectively.
See Table 3/Table 4 for slave address options.

Both pins are five-level input ports.<table><tr><td>L0</td><td>Pulled down by 1KΩ resistor</td></tr><tr><td>L1</td><td>Pulled down by 20KΩ resistor</td></tr><tr><td>L2</td><td>Left floating</td></tr><tr><td>L3</td><td>Pulled up to VDD by 20KΩ resistor</td></tr><tr><td>L4</td><td>Pulled up to VDD by 1KΩ resistor</td></tr></table></td></tr>
<tr><td>20</td><td>EQ0_ADDR0</td><td>I</td></tr>
<tr><td>18</td><td>GAIN</td><td>I</td><td>Set DC gain of equalizer.
L0: -2dB
L1: Reserve
L2: -3dB
L3: -4dB
L4: -5dB

This pin is five-level input port.<table><tr><td>L0</td><td>Pulled down by 1KΩ resistor</td></tr><tr><td>L1</td><td>Pulled down by 20KΩ resistor</td></tr><tr><td>L2</td><td>Left floating</td></tr><tr><td>L3</td><td>Pulled up to VDD by 20KΩ resistor</td></tr><tr><td>L4</td><td>Pulled up to VDD by 1KΩ resistor</td></tr></table></td></tr>
</table>

<table>
<tr>
<td>36</td>
<td>VOD</td>
<td>I</td>
<td>Set output stage driver gain.
L0: 2dB
L1: Reserve
L2: 3dB
L3: 4dB
L4: 5dB
This pin is five-level input port.
<table>
<tr><td>L0</td><td>Pulled down by 1KΩ resistor</td></tr>
<tr><td>L1</td><td>Pulled down by 20KΩ resistor</td></tr>
<tr><td>L2</td><td>Left floating</td></tr>
<tr><td>L3</td><td>Pulled up to VDD by 20KΩ resistor</td></tr>
<tr><td>L4</td><td>Pulled up to VDD by 1KΩ resistor</td></tr>
</table>
</td>
</tr>
<tr>
<td>15</td>
<td>EN_SMB</td>
<td>I</td>
<td>Set redriver configuration method.
L0: pin mode
L1: SMBus master mode
L2: SMBus slave mode
L3: I2C master mode
L4: I2C slave mode

EN_SMB = L0: redriver is configured by external strapped pins; EN_SMB = L1/L3: redriver loads settings from external EEPROM automatically after power up; EN_SMB = L2/L4: external SMBus/I2C master device configures redriver by writing settings to the registers of redriver.

EN_SMB = L1/L2, redriver adopts SMBus transaction protocol. Its optional address is listed in Table 4.
EN_SMB = L3/L4, redriver adopts I2C transaction protocol. Its optional address is listed in Table 3.

This pin is five-level input port.</td>
</tr>
</table>

			<table><tr><td>L0</td><td>Pulled down by 1KΩ resistor</td></tr><tr><td>L1</td><td>Pulled down by 20KΩ resistor</td></tr><tr><td>L2</td><td>Left floating</td></tr><tr><td>L3</td><td>Pulled up to VDD by 20KΩ resistor</td></tr><tr><td>L4</td><td>Pulled up to VDD by 1KΩ resistor</td></tr></table>
27	CLKREQB	I	Set redriver operation mode. Internally pulled down at ~150KΩ. L: normal mode H: L1.2 state
34	PWDN01	I	Enable/disable channel 0 and channel 1. Internally pulled down at ~150KΩ. L: channel 0 and channel 1 is enabled H: channel 0 and channel 1 is shut off
37	PWDN23	I	Enable/disable channel 2 and channel 3. Internally pulled down at ~150KΩ. L: channel 2 and channel 3 is enabled H: channel 2 and channel 3 is shut off
1	RX_DET	I	Set RX detection behavior. L0: far-end termination is asserted after 3x valid detections L1: far-end termination is asserted after 1x valid detections L2: far-end termination is asserted after 3x valid detections L3: far-end termination is asserted after 1x valid detections L4: far-end termination is asserted after 4x valid detections This pin is five-level input port. <table><tr><td>L0</td><td>Pulled down by 1KΩ resistor</td></tr><tr><td>L1</td><td>Pulled down by 20KΩ resistor</td></tr></table>

			L2 Left floating L3 Pulled up to VDD by 20KΩ resistor L4 Pulled up to VDD by 1KΩ resistor
I2C interface			
16	SCL	I/O	SMB/I2C interface. This interface is compatible with SMBus and I2C transaction protocol.
17	SDA	I/O	
Others			
24	CEXT1	P	Internal regulator output. Must add decoupling cap of 1uF or larger close to each pin.
31	CEXT2	P	
35	READ_EN#	I	EN_SMB = L1/L3 EEPROM load enable. When this pin is pulled low, redriver will load settings from external EEPROM automatically after power up. Internally pulled up at ~150KΩ. EN_SMB = L0/L2/L4 Reserved.
21	LOAD_DONE#	O	EEPROM load status indicator. Internally pulled up at ~150KΩ. After EEPROM loading is done successfully, this pin will output low.
28	RSV		Reserved for future use. Connect to ground with a 4.7KΩ resistor in default.
2, 38	NC		Not connected
Power pins			
5, 8, 9, 12	VDD	P	Power supply
	EPAD	G	Ground

Table 2. EQ Level Options

[EQ1, EQ0]	EQ Level	[EQ1, EQ0]	EQ Level
[L0, L0]	Base EQ (BEQ)	[L1, L0]	BEQ+5dB
[L0, L1]	BEQ+2dB	[L1, L1]	BEQ+6dB
[L0, L2]	BEQ+3dB	[L1, L2]	BEQ+7dB
[L0, L3]	BEQ+4dB	[L1, L3]	BEQ+8dB

Note: 1.Base EQ is 6dB

Table 3. I2C Slave Address Options

[ADDR1, ADDR0]	Address(8-bit, W/R)	[ADDR1, ADDR0]	Address(8-bit, W/R)
[L0, L0]	0x10/0x11	[L2, L0]	0x90/0x91
[L0, L1]	0x20/0x21	[L2, L1]	0xA0/0xA1
[L0, L2]	0x30/0x31	[L2, L2]	0xB0/0xB1
[L0, L3]	0x40/0x41	[L2, L3]	0xC0/0xC1
[L1, L0]	0x50/0x51	[L3, L0]	0xD0/0xD1
[L1, L1]	0x60/0x61	[L3, L1]	0xE0/0xE1
[L1, L2]	0x70/0x71	[L3, L2]	0xF0/0xF1
[L1, L3]	0x80/0x81	[L3, L3]	0x00/0x01

Table 4. SMBus Slave Address Options

[ADDR1, ADDR0]	Address(8-bit, W/R)	[ADDR1, ADDR0]	Address(8-bit, W/R)
[L0, L0]	0x20/0x21	[L2, L0]	0x30/0x31
[L0, L1]	0x22/0x23	[L2, L1]	0x32/0x33
[L0, L2]	0x24/0x25	[L2, L2]	0x34/0x35
[L0, L3]	0x26/0x27	[L2, L3]	0x36/0x37
[L1, L0]	0x28/0x29	[L3, L0]	0x38/0x39
[L1, L1]	0x2A/0x2B	[L3, L1]	0x3A/0x3B
[L1, L2]	0x2C/0x2D	[L3, L2]	0x3C/0x3D

[L1, L3]	0x2E/0x2F	[L3, L3]	0x3E/0x3F

ABSOLUTE MAXIMUM RATINGS

Parameters	Comments	Unit
Supply Voltage Range, VDD		-0.5V to +1.98V
Normal I/O Voltage Range		-0.5V to +1.98V
ESD	Human Body Model: Machine Model: Charged Device Model:	+/- 5000V +/- 200V +/- 2000V

ESD Standard:

Human Body Model: JS-001-2014

Machine Model: JESD22-A115-C

Charged Device Model: JS-002-2014

Latch-up Standard: EIA/JEDEC STANDARD 78E; I-Test: +/- 200mA; V-Test: 1.5X of Vcc

PACKAGE DISSIPATION RATINGS

38-pin QFN	Still air, 4-layer PCB
θ_{JA} - Junction to Ambient Thermal Resistance	48.9 °C/W
θ_{JC} - Junction to Case Thermal Resistance	21.6 °C/W
Maximum Power Dissipation Rating, Ta = 70 °C	1125mW
Maximum Power Dissipation Rating, Ta = 85 °C	818mW

NORMAL OPERATING CONDITIONS

Parameter	Conditions	MIN	TYP	MAX	Units
Supply voltage, V_{DD}		1.71	1.8	1.89	V
Ambient temperature, T_A	PS8570QFN38GTR	0		70	°C
Ambient temperature, T_A	PS8570QFN38ITR	-40		85	°C
Normal supply current, I_{NORMAL}	All four channels active		105		mA
Power saving mode current, $I_{POWER-SAVING}$			8.7		mA
Power down mode current, $I_{POWERDOWN}$	PWDN01 = H & PWDN23 = H		50		uA
L1.2 mode current, $I_{L1.2}$	CLKREQB = H			0.55	mA
Suspend mode current, $I_{suspend}$			0.55		mA
Normal operation mode power, P_{NORMAL}	All four channels active		189		mW
Power saving mode power, $P_{POWER-SAVING}$			15.7		mW
Power down mode power, $P_{POWERDOWN}$	PWDN01 = H & PWDN23 = H		90		uW
L1.2 mode power, $P_{L1.2}$	CLKREQB = H			1	mW
Suspend mode power,$P_{SUSPEND}$			1		mW

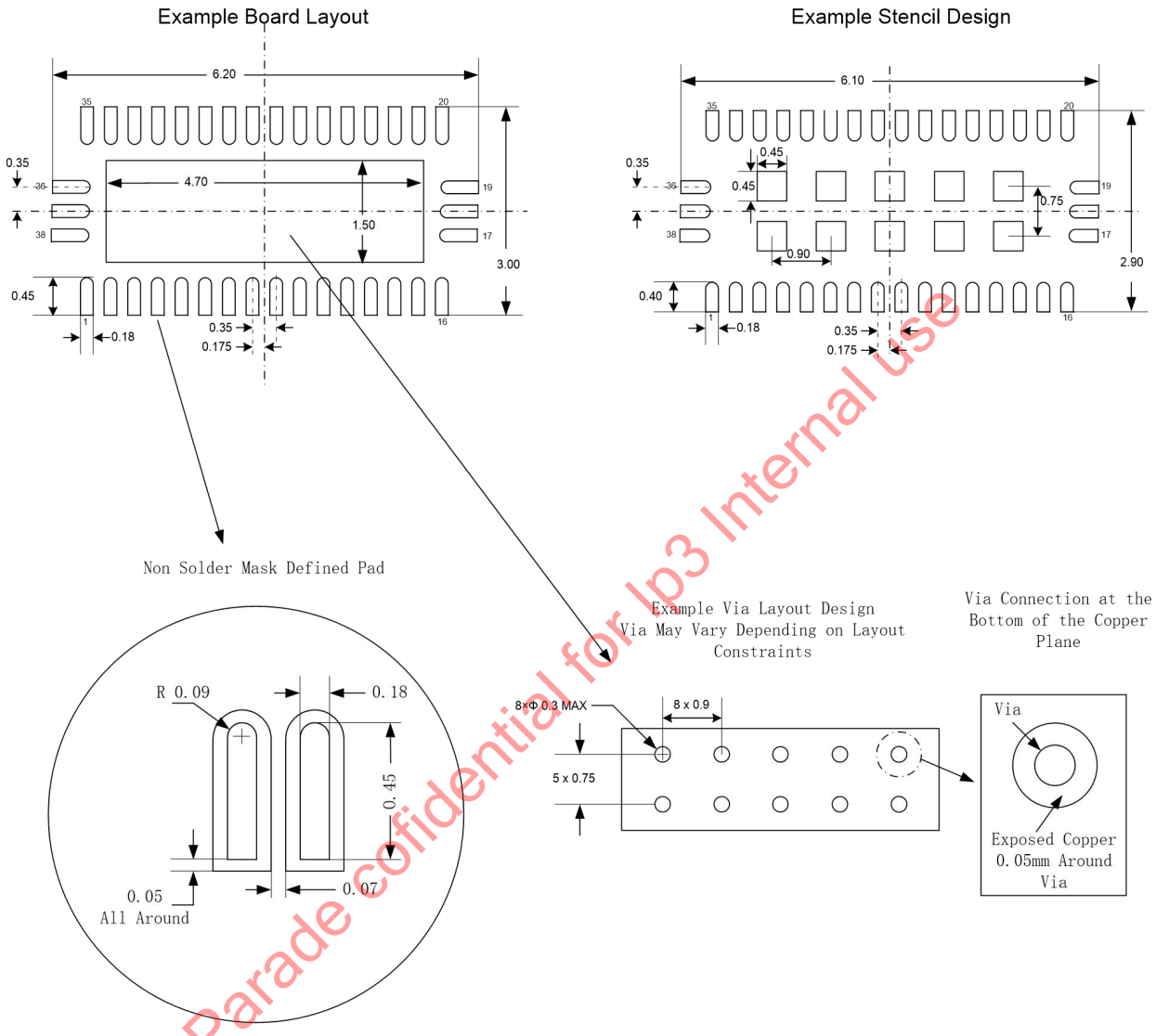
DC CHARACTERISTICS

Parameter	Conditions	MIN	TYP	MAX	Units
Two-level input pins: PWDN01, PWDN23, CLKREQB					
V_{IH} High-level input voltage V_{IL} Low-level input voltage		1.26		 0.54	V V
SCL, SDA					
V_{IH} High-level input voltage V_{IL} Low-level input voltage V_{OL} Low_level output voltage	 I_{SINK}=3mA	1.26		VDD 0.54 0.36	V V V

AC CHARACTERISTICS

Parameter	Conditions	MIN	TYP	MAX	Units
$V_{TX-DIFF}$, Differential output peak to peak voltage				1200	mV
$V_{TX-AC-CM}$, Tx AC peak-peak common mode voltage				150	mV
$V_{TX-DC-CM}$, Tx DC peak-peak common mode voltage				0.9	V
$V_{TX-IDLE-DIFF-AC}$, AC electrical idle differential peak output voltage				20	mV
$V_{TX-IDLE-DIFF-DC}$, DC electrical idle differential peak output voltage				5	mV
C_{TX}, AC coupling capacitor		176		265	nF
$Z_{TX-DIFF-DC}$, Tx DC differential impedance				120	Ω
$R_{RX-DIFF-DC}$, Rx DC differential impedance			100		Ω

$V_{RX-IDLE-DET-DIFF-PP}$, Electrical idle detect threshold		65		175	mV



NOTES:

1. All dimensions are in millimeters.
2. The drawing is subject to change without notice.
3. Customers should contact their board fabrication site for recommend solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

Figure 4. Exposed Thermal Pad Layout Guidelines for PS8570

ORDERING & PACKAGING INFORMATION – Commercial Application

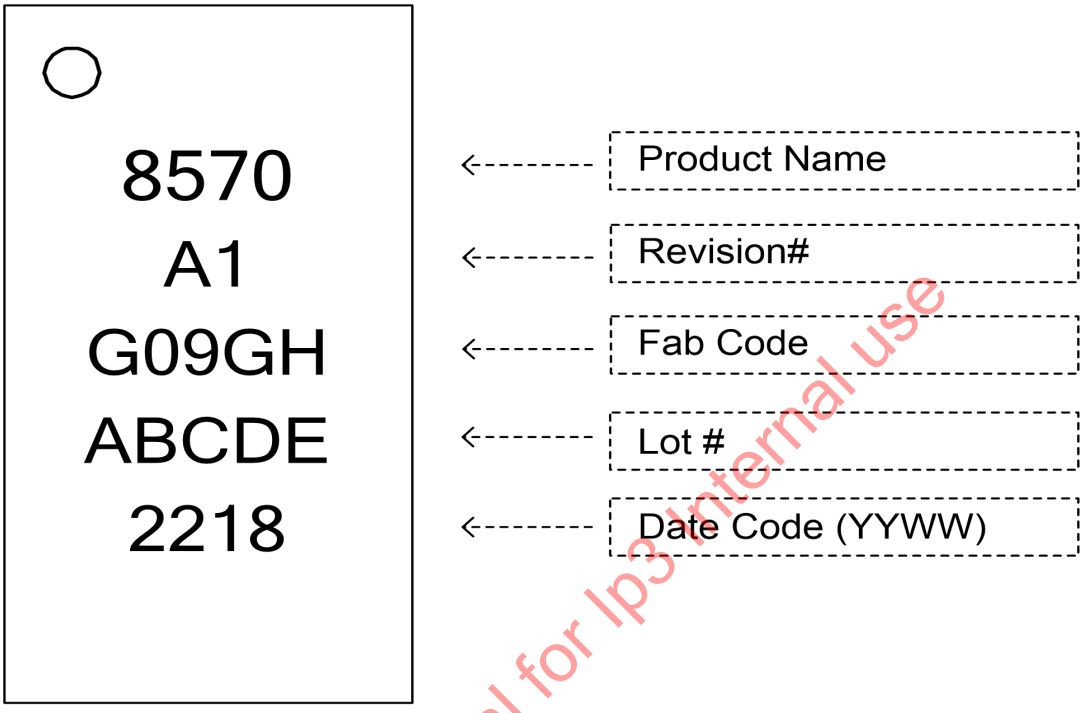
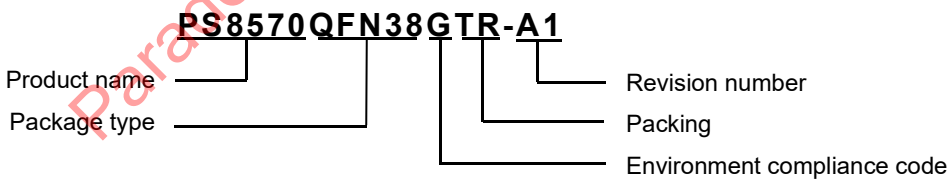


Figure 5. Top Side Marking – Commercial Version

Ordering Information

PS8570 part number:



Part Number	Packing
PS8570QFN38GTR-A1	Tape and Reel

Lead Finish: 100% Sn

ORDERING & PACKAGING INFORMATION – Industrial Application

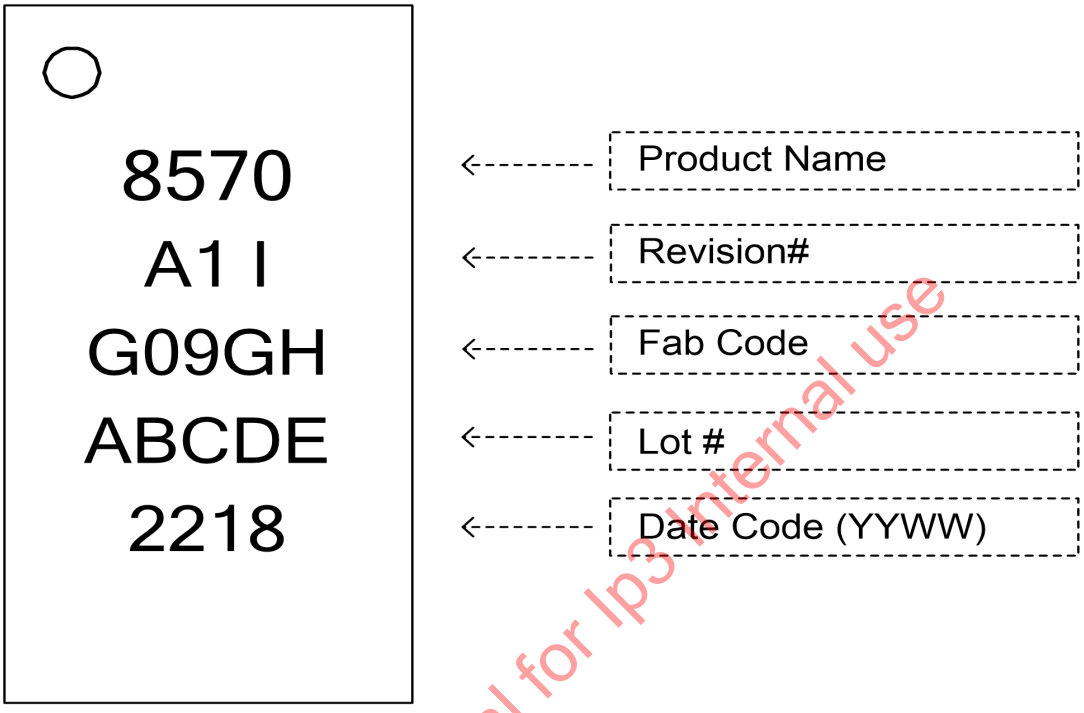
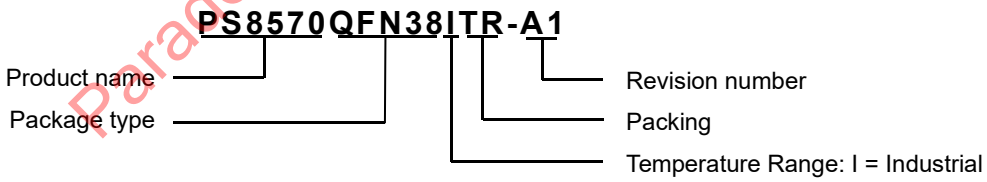


Figure 6. Top Side Marking – Industrial Version

Ordering Information

PS8570 part number:



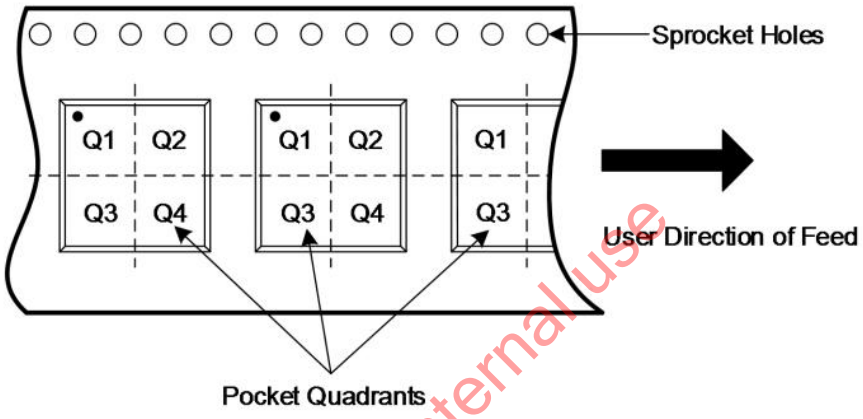
Part Number	Packing
PS8570QFN38ITR-A1	Tape and Reel

Lead Finish: 100% Sn

TAPE AND REEL PACKING PIN1 ORIENTATION

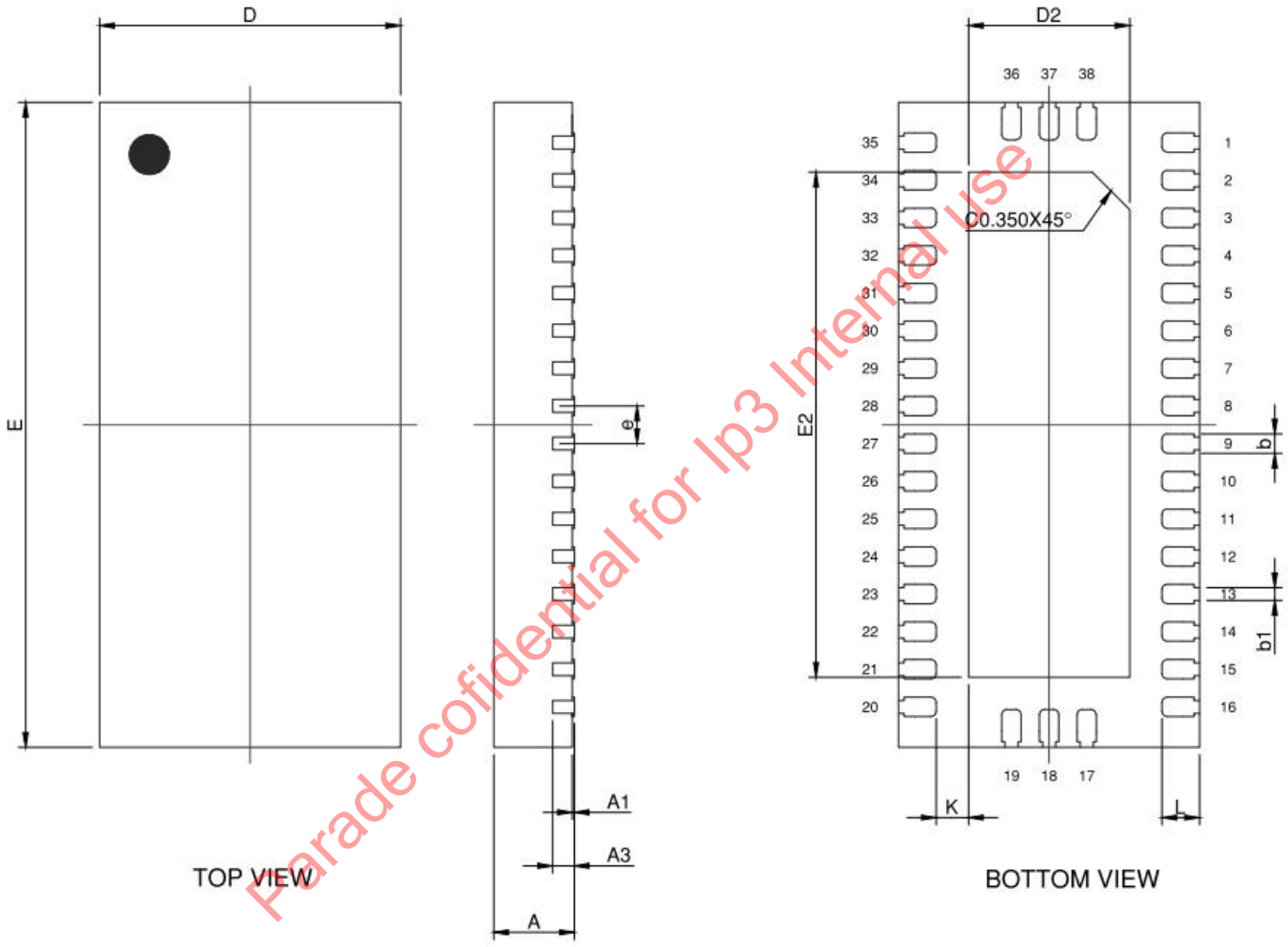
TR
(EIA conforming)

QUADRANT ASSIGNMENT FOR PIN1 ORIENTATION IN TAPE



PHYSICAL DIMENSION

38-pin QFN: 2.8 x 6 mm²



Parameter	MIN	NOM	MAX	Unit
A	0.70	0.75	0.80	mm
A1	0.00	0.02	0.05	mm
A3		0.203 REF		mm
b	0.13	0.18	0.23	mm
b1		0.120 REF		mm
D	2.70	2.80	2.90	mm
E	5.90	6.00	6.10	mm
e		0.35 BSC		mm
L	0.30	0.35	0.40	mm
D2	1.45	1.50	1.55	mm
E2	4.65	4.70	4.75	mm
K	0.20	-	-	mm

REVISION HISTORY

Version	Date	Items
0.6	2022/04/20	Initial release
0.7	2022/08/31	1. Update I2C address 2. Update ESD data 3. Update power data
0.71	2023/04/21	1. Update part number to A1